In the Specification:

Please amend paragraph 0024, line 3 as follows:

If the method of FIG. 2 is selected in step 44 then step 46 is executed such that the film layer 21 (see FIG. 2) is removed from the wafer 4 thereby exposing the film layer [[21]] 24 (coupled to the semiconductor wafer 4) to the topside 12 of the semiconductor wafer 7. In step 56 the wafers 4 and 7 are placed in a furnace for wafer/semiconductor device manufacturing process thereby producing a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7.